In the claims

Please amend the claims as follows:

1. (Currently Amended) A resistance calibration circuit for use in a semiconductor device comprising:

a correction code generating means for generating a plurality of push-up code signals ~~and a plurality of pull-down code signals based on an external reference resistor, wherein a reference voltage is applied to the correction code generating means~~ based on a comparison result between a voltage applied to an external reference resistor and a reference voltage and for generating a plurality of pull-down code signals based on the plurality of push-up code signals and the reference voltage;

a push-up decoder for decoding the plurality of push-up code signals ~~from the correction code generating means~~ to thereby generate a plural-bit push-up signal;

a pull-down decoder for decoding the plurality of pull-down code signals ~~from the correction code generating means~~ to thereby generate a plural-bit pull-down signal; and

a resistance adjustor ~~for receiving a push-up signal from the push-up decoder and a pull-down signal from the pull-down decoder and~~ for selectively turning on/off a plurality of inner transistors included in the resistance adjustor according to the plural-bit push-up signal and the plural-bit pull-down signal.

2. (Currently Amended) The resistance calibration circuit in accordance with claim 1, wherein the correction code generating means includes:

a first OP amplifier for comparing ~~a~~ the voltage applied to the external reference resistor with ~~a~~ the reference voltage ~~applied to a second input terminal, outputting~~ in order to output a first logic level if the voltage applied to the ~~first input terminal~~ external reference resistor is higher than the reference voltage~~, and outputting~~ and output a second logic level if the voltage applied to the ~~first input terminal~~ external reference resistor is lower than the reference voltage;

a first calculating means for ~~producing the push-up code signals using an input signal from the first OP amplifier~~ generating the plurality of push-up code signals according to an

output of the first OP amplifier;

a first p-type metal oxide semiconductor (PMOS) transistor group having a plurality of PMOS transistors, each of which has a gate to receive one of the push-up code signals and a source connected to a power supplier;

a first resistor connected ~~to~~ between drains of the first PMOS transistor group and ~~the~~ a first input terminal of the first OP amplifier;

a second PMOS transistor group having a plurality of PMOS transistors, each of which has a gate to receive one of the push-up code signals and a source connected to the power supplier;

a second resistor connected to drains of the second PMOS transistor group;

a second OP amplifier of which first input terminal is connected to the second resistor, wherein the second OP amplifier compares a voltage applied to ~~a~~ the first input terminal with the reference voltage ~~applied to a second input terminal, outputs~~ in order to output the first logic level if the voltage applied to the first input terminal is higher than the reference voltage and ~~outputs~~ output the second logic level if the voltage applied to the first input terminal is lower than the reference voltage;

a second calculating means for ~~producing the pull-down code signals using an input signal from the second OP amplifier~~ generating the plurality of pull-down code signals according to an output of the second OP amplifier;

a first n-type metal oxide semiconductor (NMOS) transistor group having a plurality of NMOS transistors, each of which has a gate to receive one of the pull-down code signals and a source connected to ~~the power supplier~~ a ground voltage;

a third resistor connected ~~to~~ between drains of the first NMOS transistor group and ~~a~~ the first input terminal of the second OP amplifier; and

a controller coupled to the first and the second calculating means for controlling the first and the second calculating means.

3. (Currently Amended) The resistance calibration circuit in accordance with claim 2, wherein the push-up decoder includes:

a first NAND gate for ~~NANDing~~ performing a logic NAND operation on first and second enable signals;

a first NOR gate for ~~NORing~~ performing a logic NOR operation on a first push-up code signal and an output ~~signal from~~ of the first NAND gate;

a second NOR gate for ~~NORing~~ performing a logic NOR operation on a second push-up code signal and the output ~~signal from~~ of the first NAND gate;

a third NOR gate for ~~NORing~~ performing a logic NOR operation on a third push-up code signal and the output ~~signal from~~ of the first NAND gate to thereby output a fourth bit of the plural-bit push-up signal;

a fourth NOR gate for ~~NORing~~ performing a logic NOR operation on ~~output signals from the first and second NOR gates~~ an output of the first NOR gate and an output of the second NOR gate;

a first inverter for inverting ~~an output signal from~~ the output of the first NOR gate;

a second inverter for inverting ~~an output signal from~~ the output of the second NOR gate;

a third inverter for inverting an output ~~signal from~~ of the third NOR gate;

a second NAND gate for ~~NANDing~~ performing a logic NAND operation on ~~output signals from the first and second NOR gates~~ the output of the first NOR gate and the output of the second NOR gate;

a fifth NOR gate for ~~NORing~~ performing a logic NOR operation on output signals ~~from~~ of the first to the third inverters ~~and outputting~~ to thereby output a first bit of the plural-bit push-up signal;

a sixth NOR gate for ~~NORing~~ performing a logic NOR operation on output signals ~~from~~ of the second and the third inverters ~~and outputting~~ to thereby output a second bit of the plural-bit push-up signal;

a seventh NOR gate for ~~NORing~~ performing a logic NOR operation on an output ~~signal from~~ of the fourth NOR gate and ~~an output signal from~~ the output of the third inverter ~~and outputting~~ to thereby output a third bit of the plural-bit push-up signal~~, wherein the third NOR gate outputs a fourth bit of the push-up signal by NORing a third push-up code signal and the output signal from the first NAND gate~~;

a third NAND gate for ~~NANDing~~ performing a logic NAND operation on an output ~~signal from~~ of the second NAND gate and the output ~~signal from~~ of the third inverter ~~and outputting~~ to thereby output a fifth bit of the plural-bit push-up signal;

a fourth NAND gate for ~~NANDing~~ performing a logic NAND operation on ~~output~~

~~signals from the second and third inverters~~ the output of the second inverter and the output of the third inverter ~~and outputting~~ to thereby output a sixth bit of the plural-bit push-up signal;

a fifth NAND gate for ~~NANDing~~ performing a logic NOR operation on output signals ~~from~~ of the first to the third inverters ~~and outputting~~ to thereby output a seventh bit of the plural-bit push-up signal; and

a fourth inverter for inverting ~~an output signal from~~ the output of the first NAND gate ~~and outputting~~ to thereby output an eighth bit of the plural-bit push-up signal.

4. (Currently Amended) The resistance calibration circuit in accordance with claim 3, wherein the pull-down decoder includes:

a sixth NAND gate for ~~NANDing~~ performing a logic NAND operation on the first and the second enable signals to thereby output an eighth bit of the plural-bit pull-down code signal;

an eight NOR gate for ~~NORing~~ performing a logic NOR operation on a first pull-down code signal and an output ~~signal from~~ of the sixth NAND gate;

a ninth NOR gate for ~~NORing~~ performing a logic NOR operation on a second pull-down code signal and the output ~~signal from~~ of the sixth NAND gate;

a tenth NOR gate for ~~NORing~~ performing a logic NOR operation on a third push-up code signal and the output ~~signal from~~ of the sixth NAND gate;

a fifth inverter for inverting an output ~~signal from~~ of the eight NOR gate;

a sixth inverter for inverting an output ~~signal from~~ of the ninth NOR gate;

a seventh inverter for inverting an output ~~signal from~~ of the tenth NOR gate to thereby output a fourth bit of the plural-bit pull-down signal;

a seventh NAND gate for ~~NANDing~~ performing a logic NAND operation on ~~output signals from the fifth and sixth inverters~~ an output of the fifth inverter and an output of the sixth inverter;

an eight inverter for inverting ~~an output signal from~~ the output of the fifth inverter;

a ninth inverter for inverting ~~an output signal from~~ the output of the sixth inverter;

a tenth inverter for inverting an output ~~signal from~~ of the seventh inverter;

an eleventh NOR gate for ~~NORing~~ performing a logic NOR operation on ~~output signals from the fifth and sixth inverters~~ the output of the fifth inverter and the output of the sixth inverter;

an eight NAND gate for ~~NANDing~~ performing a logic NAND operation on output signals ~~from~~ of the eight to the tenth inverters ~~and outputting~~ to thereby output a first bit of the plural-bit pull-down signal;

a ninth NAND gate for ~~NANDing~~ performing a logic NAND operation on ~~output signals from the ninth and tenth and tenth inverters and outputting~~ the output of the ninth inverter and the output of the tenth inverter to thereby output a second bit of the plural-bit pull-down signal;

a tenth NAND gate for ~~NANDing~~ performing a logic NAND operation on ~~output signals from the seventh NAND gate and the tenth inverter and outputting~~ an output of the seventh NAND gate and the output of the tenth inverter to thereby output a third bit of the plural-bit pull-down signal~~, wherein the seventh inverter outputs a fourth bit of the pull-down signal by inverting an output signal from the tenth NOR gate~~;

a twelfth NOR gate for ~~NORing~~ performing a logic NOR operation on ~~output signals from the eleventh NOR gate and the tenth inverter and outputting~~ an output of the eleventh NOR gate and the output of the tenth inverter to thereby output a fifth bit of the plural-bit pull-down signal;

a thirteenth NOR gate for ~~NORing~~ performing a logic NOR operation on ~~output signals from the ninth to tenth inverters and outputting~~ the output of the ninth inverter and the output of the tenth inverter to thereby output a sixth bit of the plural-bit pull-down signal; and

a fourteenth NOR gate for ~~NORing~~ performing a logic NOR operation on ~~output signals from the eight to tenth inverters and outputting~~ the output signals of the eighth to the tenth inverters to thereby output a seventh bit of the plural-bit pull-down signal~~, wherein the sixth DAND gate outputs an eighth bit of the pull-down signal by NANDing the first and second enable signals~~.

5. (Currently Amended) The resistance calibration circuit in accordance with claim 4, wherein the resistance adjustor includes:

a third PMOS transistor group having a plurality of PMOS transistors, each of which has a gate ~~to receive~~ coupled to one bit of the plural-bit push-up signal~~,~~ and a source connected to the power supplier;

a fourth resistor connected to drains of the third PMOS transistor group and an I/O terminal thereof;

a second NMOS transistor group having a plurality of NMOS transistors, each of which has a gate ~~to receive~~ coupled to one bit of the plural-bit pull-down signal~~,~~ and a source connected to a ground voltage level; and

a fifth resistor connected to drains of the second NMOS transistor group and the I/O terminal thereof.

6. (Original) A resistance calibration circuit in a semiconductor device, wherein the resistance calibration circuit is coupled to an I/O terminal of the semiconductor device, the resistance calibration circuit comprising;

a first resistor connected to the I/O terminal;

a second resistor connected to the I/O terminal;

a plurality of push-up transistors connected to the first resistor and controlled by a push-up signal, wherein the push-up transistors are in parallel connected to each other;

a plurality of pull-down transistors connected to the second resistor and controlled by a pull-down signal, wherein the pull-down transistors are in parallel connected to each other; and

a control signal generator for producing the push-up signal and the pull-down signal based on a voltage variation of a voltage difference between a reference voltage and an external voltage, wherein the external voltage is applied to a fixed resistor.

7. (Original) The resistance calibration circuit in accordance with claim 6, wherein the control signal generator includes:

a correction code generating means for generating a plurality of push-up code signals and a plurality of pull-down code signals based on an external reference resistor, wherein a reference voltage is applied to the correction code generating means;

a push-up decoder for decoding the plurality of push-up code signals from the correction code generating means;

a pull-down decoder for decoding the plurality of pull-down code signals from the correction code generating means; and

a resistance adjustor for receiving a push-up signal from the push-up decoder and a pull-down signal from the pull-down decoder and for turning on/off a plurality of inner transistors.

COMMENTS

Reconsideration and allowance in view of the following amendments and the following remarks are respectfully requested.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Otsuka (U.S.P. 6,466,487). Applicant respectfully traverses the rejection for the following reasons.

Applicant asserts that the cited reference does not disclose, teach or suggest all the features of the present invention.

According to the present invention, the push-up code signal is generated by comparing the voltage applied to the external reference resistor with the reference voltage. Then, contrary to the cited reference, the pull-down code signal is generated based on the generated push-up code signal and the reference voltage (see Fig.2, lines 1 to 13 on page 6 and line 20 on page 6 to line 11 on page 7). That is, the pull-up resistance is firstly adjusted according to the voltage applied to the external reference resistor and the reference voltage, and then the pull-down resistance is adjusted according to the adjusted pull-up resistance. Accordingly, the pull-down resistance is dependent upon the push-up resistance (see lines 18 and 19 on page 13) as recited in Claims 1, lines 13-16.

However, according to Otsuka, the counters (224 and 225) independently and respectively generate the data pieces D0 to Dn-1 and U0 to Um-1 (see FIG. 8). That is, each of the OP amplifiers OP2 and OP3 receives the voltage applied to the external resistor, i.e., VZQ applied to RQ, and one of the reference voltages (REFIU and REFID) for comparing them to thereby generate the data pieces D0 to Dn-1 and U0 to Um-1. However, according to the present invention, only one of the OP amplifiers (201 and 207) receives both the reference voltage and the voltage loaded on the external resistor and the other amplifiers do not receive the voltage loaded on the external resistor. Please note that Otsuka fails to disclose or suggest using output of one of the counters for controlling the other of the counters.

Accordingly, Applicant believes that all claims are now patentable over the cited reference issued by the Examiner.

If there are any fees due in connection with the filing of this response, please charge

those fees to our Deposit Account No. 02-2666. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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Dated: January 14, 2005

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Linda Marie D'Elia January 14, 2005

ESH/lmd